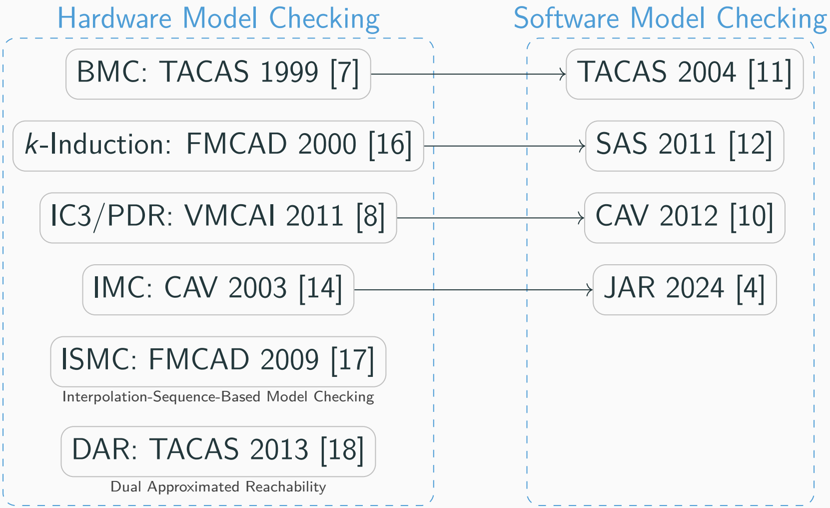
A Transferability Study of Interpolation-Based Hardware Model Checking for Software Verification

Dirk Beyer, **Po-Chun Chien**, Marek Jankola, and Nian-Ze Lee

CPA 2024 @ Milan, Italy
LMU Munich, Germany

Motivation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Software Model Checking
BMC: TACAS 1999 [7]
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k-Induction: FMCAD 2000 [16]
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DAR: TACAS 2013 [18]
Dual Approximated Reachability

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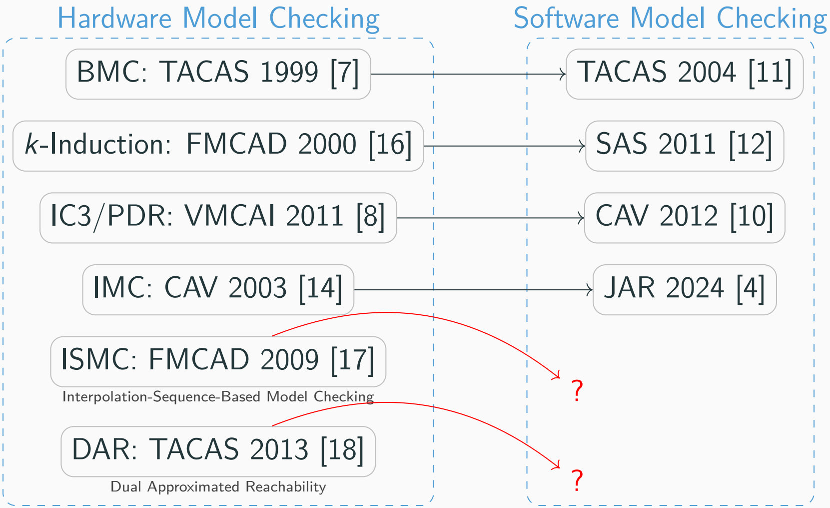
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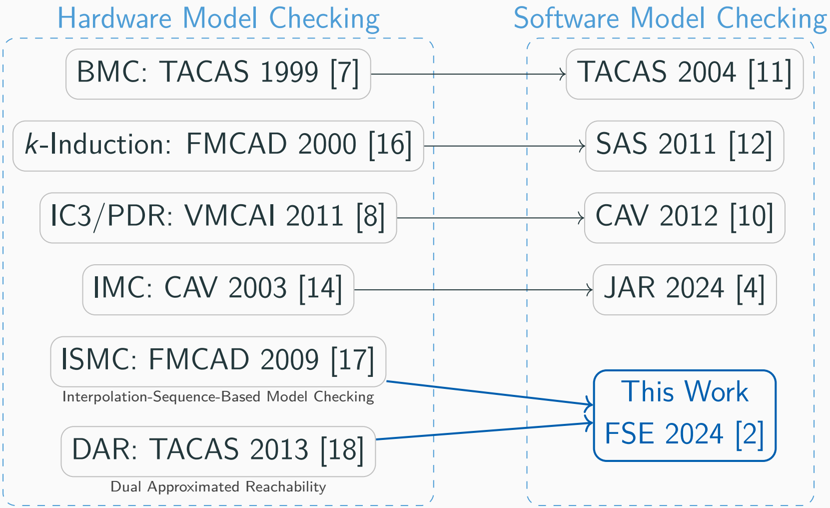
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This Work
FSE 2024 [2]
DAR: TACAS 2013 [18]
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Highlights

- First systematic study on the transferability of hardware model checking
- For software verification
  - ISMC and DAR are useful
  - Evaluation confirms that algorithmic characteristics remain

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- For software verification
  - ISMC and DAR are useful
  - Evaluation confirms that algorithmic characteristics remain
- Open-source implementation of ISMC and DAR in CPAchecker
- Reproduction package available on Zenodo [1]

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1. Background
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- Safety property: $P(s)$

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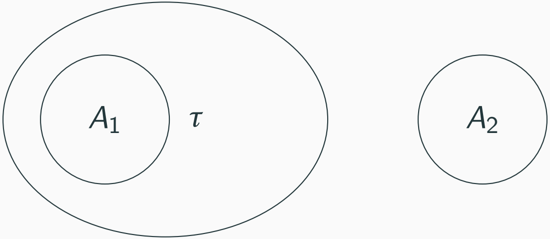
  - if SAT, counterexample found
  - if UNSAT, no counterexample at bound k
    → compute abstraction using *interpolation*

Craig Interpolation

- If $A_1(X,Y) \wedge A_2(Y,Z)$ is UNSAT: interpolant $\tau(Y)$
  - $A_1(X,Y) \Rightarrow \tau(Y)$ is valid
  - $\tau(Y) \wedge A_2(Y,Z)$ is UNSAT



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IMC (McMillan 2003 [14])

- At unrolling bound k:
  $Init(s_0)\,T(s_0,s_1)\;T(s_1,s_2)\ldots T(s_{k-1},s_k)(\neg P(s_1)\vee\ldots\vee\neg P(s_k))$

IMC (McMillan 2003 [14])

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  $$\underbrace{Init(s_0)\,T(s_0,s_1)}_{A_1(s_0,s_1)}\;\underbrace{T(s_1,s_2)\ldots T(s_{k-1},s_k)(\neg P(s_1)\vee\ldots\vee\neg P(s_k))}_{A_2(s_1,s_2,\ldots,s_k)}$$
  - Interpolant $\tau_1(s_1)$: 1-step safe overapproximation

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- $$\underbrace{\tau_1(s_0)\,T(s_0,s_1)}_{A'_1(s_0,s_1)}\,\underbrace{T(s_1,s_2)\ldots T(s_{k-1},s_k)(\neg P(s_1)\vee\ldots\vee\neg P(s_k))}_{A_2(s_1,s_2,\ldots,s_k)}$$
  - Interpolant $\tau_2(s_1)$: 2-step safe overapproximation

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  - Interpolant $\tau_1(s_1)$: 1-step safe overapproximation
- $$\underbrace{\tau_1(s_0)\,T(s_0,s_1)}_{A_1'(s_0,s_1)}\ \underbrace{T(s_1,s_2)\ldots T(s_{k-1},s_k)(\neg P(s_1)\vee\ldots\vee\neg P(s_k))}_{A_2(s_1,s_2,\ldots,s_k)}$$
  - Interpolant $\tau_2(s_1)$: 2-step safe overapproximation
  - Derive τ_n iteratively until $\bigvee_{i=1}^{n}\tau_i$ reaches a fixed point

ISMC (Vizel and Grumberg, 2009 [17])

- Forward reachability sequence: $\langle R_1, R_2, \ldots, R_k = \top \rangle$
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  - Interpolation sequence $\langle \tau_1^k, \tau_2^k, \ldots, \tau_k^k \rangle$: 1- to k-step overapproximations

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  - Check if $\bigvee_{i=1}^{k} R_i'$ is a fixed point

DAR (Vizel, Grumberg, and Shoham, 2013 [18])

- Forward *and backward* reachability sequences
  - $\overline{F} = \langle F_0 = \mathit{Init}, F_1, F_2, \ldots, F_k \rangle$: forward reachability from *Init*
  - $\overline{B} = \langle B_0 = \neg P, B_1, B_2, \ldots, B_k \rangle$: backward reachability from $\neg P$

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  - If $F_i \wedge T \wedge B_{k-i}$ is UNSAT: no counterexample within $k+1$ steps

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  - Compute interpolation sequence to refine and extend $\overline{F}$ (similar to ISMC)
- Until $\overline{F}$ or $\overline{B}$ reaches a fixed point

Conceptual Differences between IMC, ISMC, and DAR

	Fixed Point	Reuse Interpolants	Local/Global Queries
IMC	$\bigvee_i \tau_i$	No	Global
ISMC	$\bigvee_i R_i$	Yes	Global
DAR	$\bigvee_i F_i$ or $\bigvee_i B_i$	Yes	Local + Global

Local/Global: query involves one/multiple transition(s)

Adoption for Software Reachability Checking

- Implement IMC, ISMC, and DAR in CPAchecker
- Use *large-block encoding* [3] to obtain transition relations
- Encode program semantics as SMT formulas (bit-precise theories)
- Employ MathSAT5 [9] for SMT solving and interpolation

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Steps

- Extract findings/claims from original papers of ISMC and DAR
  - Run-time efficiency and effectiveness
  - Algorithmic characteristics: #unrollings, #interpolants, ...
  - Comparisons with IMC
- Perform experiments to validate these findings

ISMC vs. IMC

Findings in original paper [17]	Our study
H1.A: ISMC is faster at finding bugs	✓
H1.B: ISMC proves property faster at high unrolling bounds	
H1.C: ISMC is overall faster	

DAR vs. IMC

Findings in original paper [18]	Our study
H2.A: DAR performs more local than global strengthenings	✓
H2.B: DAR is faster at proving property	
H2.C: DAR computes more interpolants	✓
H2.D: DAR's run-time is more sensitive to sizes of interpolants	
H2.E: DAR is overall faster	

Differences in Experimental Settings

		Ours [2]	ISMC [17]	DAR [18]
	Platform	CPAchecker	Intel's tool	Cadence's Jasper
	Solver	MathSAT5 (SMT)	Eureka (SAT)	SAT solver
Benchmark set	Type	C program	HW circuit	HW circuit
	Source	AWS-C-Comm., Linux, ...	Intel CPUs	Industrial designs
	#safe	6 020	69	37
	#unsafe	2 793	67	≥ 4
Limit	Time	1 800 s	10 000 s	1 800 s
	Memory	15 GB	N/A	N/A

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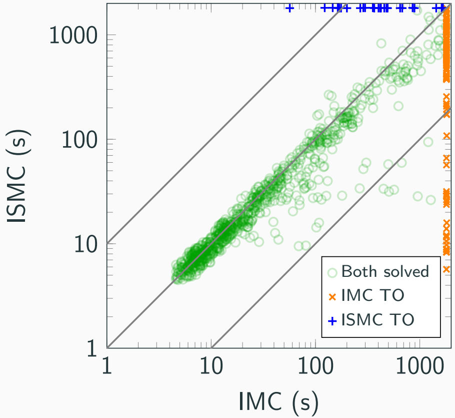
Evaluation: ISMC vs. IMC

H1.A: ISMC is faster than IMC at finding property violations ✓

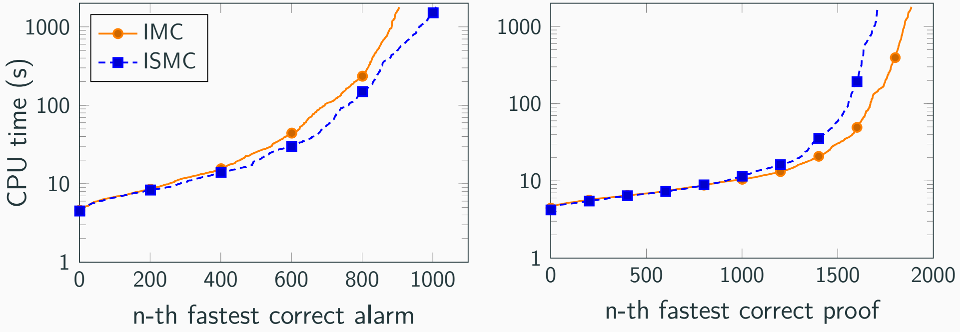


- Both solved: 873
- Accumulated CPU time

ISMC: 67 300 s
IMC: 93 300 s
Ratio: 0.72

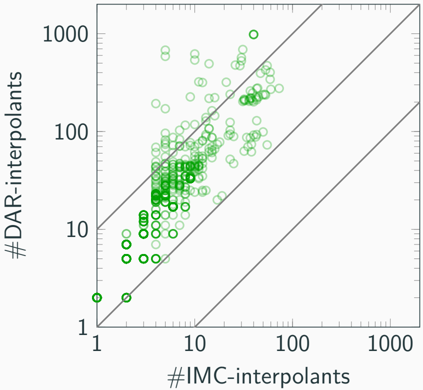
Evaluation: ISMC vs. IMC

H1.C: Overall, ISMC is faster than IMC (by 30 % in the original publication). ?



Evaluation: DAR vs. IMC

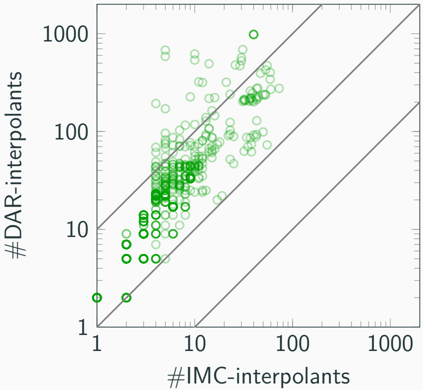
H2.C: DAR computes more interpolants than IMC. ✓

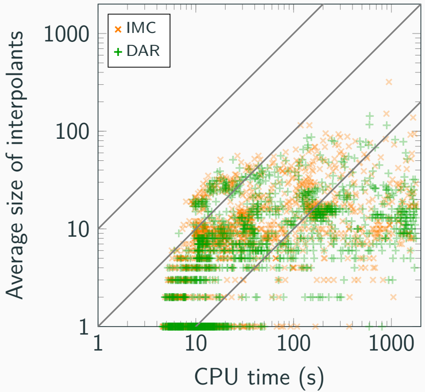


Evaluation: DAR vs. IMC

H2.C: DAR computes more interpolants than IMC. ✓

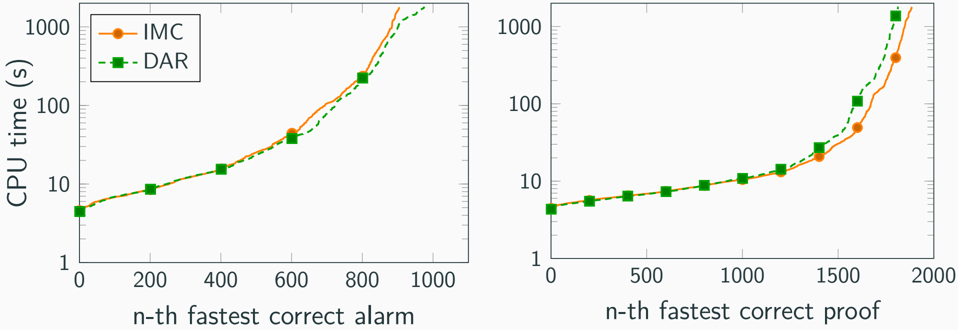
H2.D: DAR's run-time is more sensitive to the sizes of interpolants than IMC. ?





Evaluation: DAR vs. IMC

H2.E: Overall, DAR is faster than IMC (by 36% in the original publication). ?



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Conclusion

- A systematic study on the transferability of hardware model checking
- Revisiting previous literature is oftentimes fruitful
- ISMC and DAR are useful additions to software-verification methods

doi: 10.1145/3660797

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