Bridging Hardware and Software Formal Verification

Po-Chun Chien

SoSy-Lab, LMU Munich

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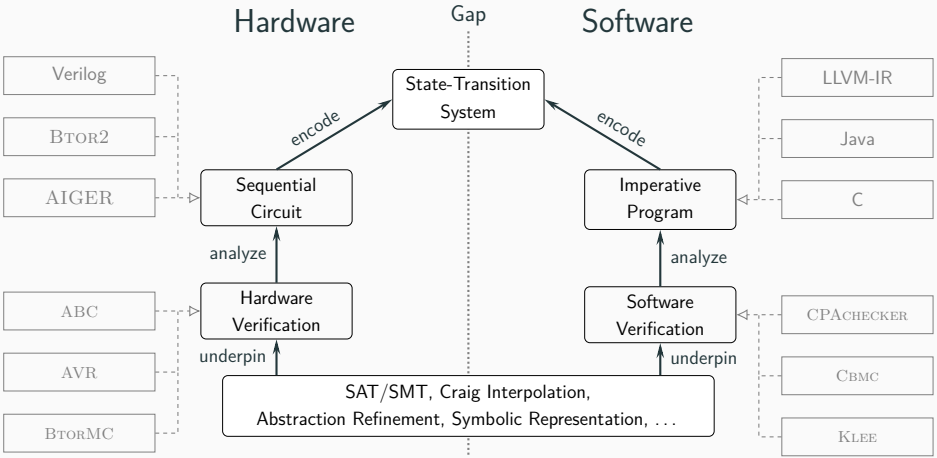
SoSy-Lab
Software Systems

LMU LUDWIG-MAXIMILIANS-UNIVERSITÄT MÜNCHEN

Motivation


Hardware
Gap
Software
Verilog
Btor2
AIGER
State-Transition System
encode
encode
LLVM-IR
Java
C
Sequential Circuit
Imperative Program
analyze
analyze
ABC
AVR
BtorMC
Hardware Verification
Software Verification
CPAchecker
Cbmc
Klee
underpin
underpin
SAT/SMT, Craig Interpolation,
Abstraction Refinement, Symbolic Representation, ...

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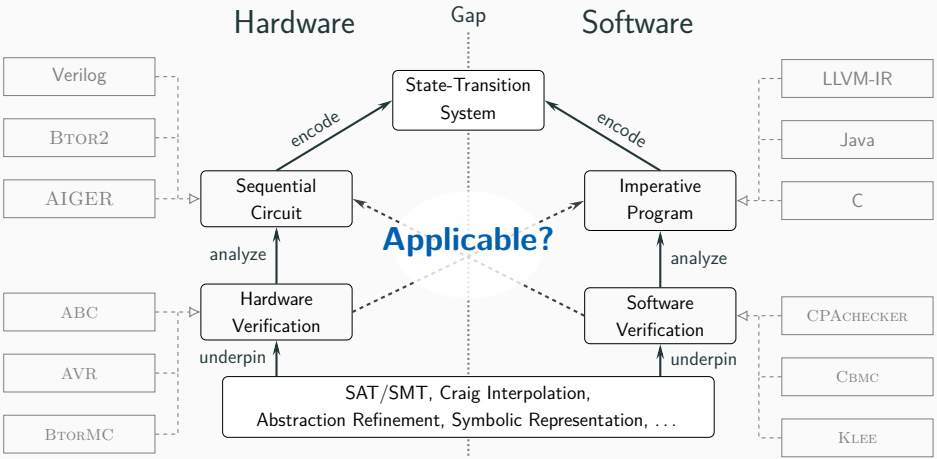
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Translating Verification Tasks

- BTOR2-CERT [1]
  BTOR2-to-C translation by BTOR2C [3]
- CPV [11]
  C-to-BTOR2 translation by KRATOS2 [16]

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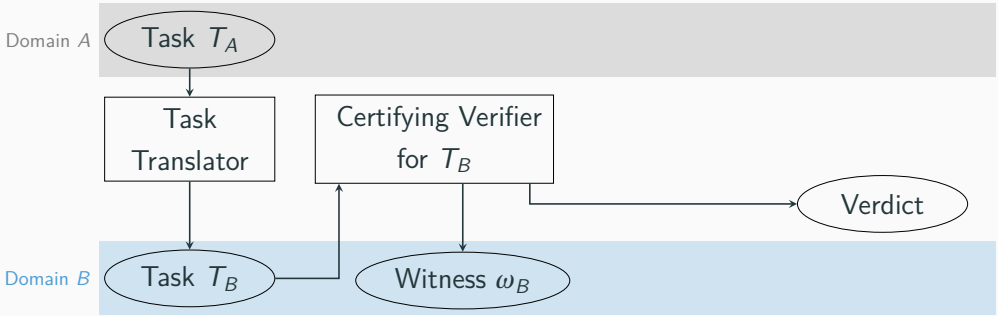

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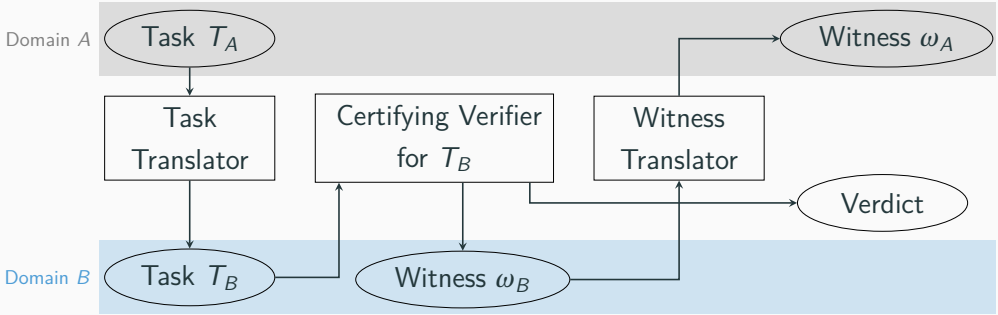
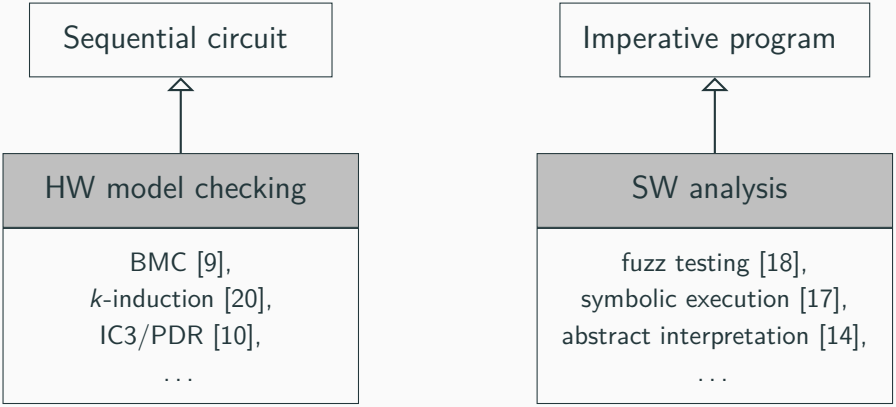


Transferring Verification Techniques Across Domains



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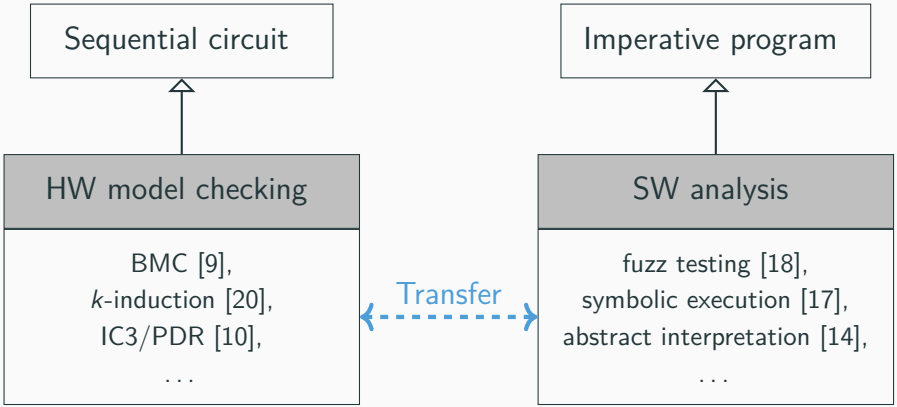
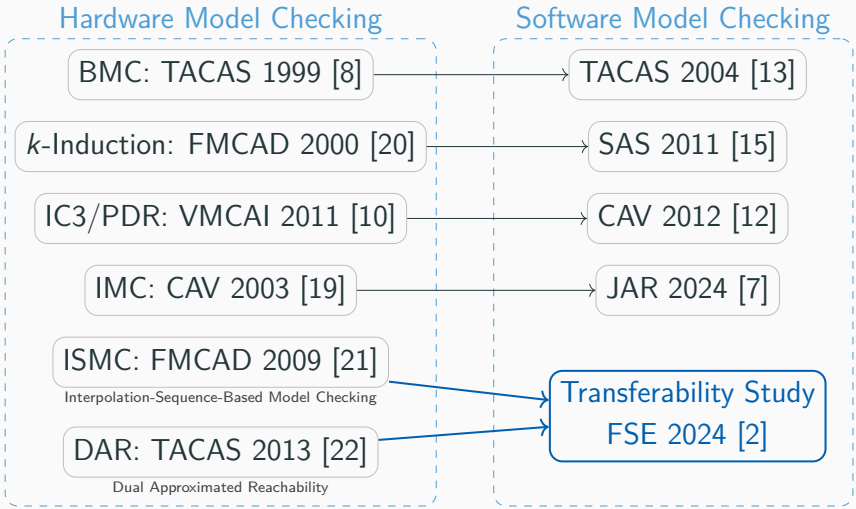


Verification Algorithm Adoption



Joing Forces of Hardware and Software Verification

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- Strengthen Craig interpolants with auxiliary invariants [5]
- Augmented vs. plain IMC
  - Improve effectiveness
  - Reduce elapsed wall-time

Data Availability and Reproducibility

- Tools available on `gitlab.com/sosy-lab/software/`



BTOR2-CERT [1] CPV [11] CPACHECKER [6]

- Research artifacts available on Zenodo

Conclusion

- Transformation between different representations to leverage their unique strengths
- Cooperative and cross-disciplinary approaches are beneficial
- Ultimate goal:
  - HW/SW co-verification
  - Tackle more complex heterogeneous systems

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